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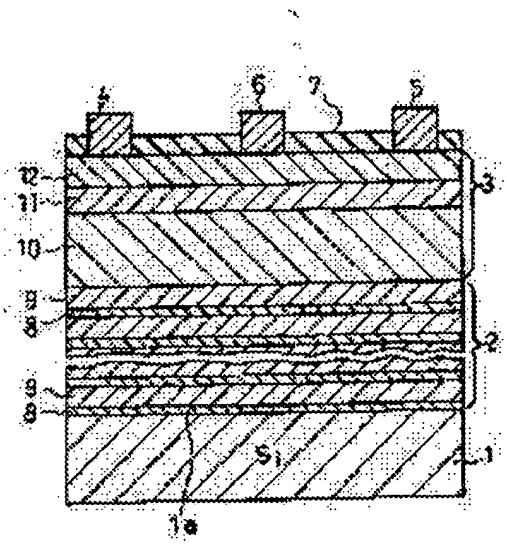
(54) SEMICONDUCTOR DEVICE AND PRODUCTION METHOD THEREFOR

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the costs of a GaN compound semiconductor device.

SOLUTION: A buffer layer 2 is provided with the structure of alternately laminating a plurality of first layers 8 composed of Al and second layers 9 composed of GaN on a wafer 1 composed of silicon. A gallium-nitride semiconductor region 3 for HEMT element is formed on the buffer layer 2.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The substrate which is the semiconductor device which has a nitride system compound semiconductor, and consists of silicon or a silicon compound, The semiconductor region for semiconductor devices containing at least one nitride system compound semiconductor layer which has been arranged on one principal plane of said substrate, and has been arranged on a buffer layer and said buffer layer, the 1st main electrode, 2nd main electrode, and control electrode which have been arranged on the front face of said semiconductor region for semiconductor devices -- having -- said buffer layer -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which it is here and said

前記x及びyは、 $0<x\leqq 1$、
$0\leqq y<1$、
$x+y\leqq 1$

M was chosen from In (indium) and B (boron),

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula AlaMbGa1-a-bN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

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the numeric value to satisfy and the semiconductor device which comes out and is characterized by consisting of a compound layer with the 2nd layer which consists of the ingredient shown.
[Claim 2] It is the semiconductor device according to claim 1 characterized by for said 1st layer consisting of AlxGa1-xN, and said 2nd layer consisting of AlaGa1-aN.
[Claim 3] It is the semiconductor device according to claim 1 characterized by for said 1st layer consisting of AlxInyGa1-x-yN, and for said 2nd layer consisting of AlaInbGa1-a-bN, and containing In (indium) at least in one side of said 1st and 2nd layers.
[Claim 4] It is the semiconductor device according to claim 1 characterized by for said 1st layer consisting of AlxByGa1-x-yN, and for said 2nd layer consisting of AlaBbGa1-a-bN, and containing B (boron) at least in one side of said 1st and 2nd layers.
[Claim 5] Said buffer layer is a semiconductor device according to claim 1, 2, 3, or 4 characterized by consisting of said two or more 1st and 2nd layers, and carrying out the laminating of said the 1st layer and said 2nd layer by turns.
[Claim 6] A semiconductor device claim 1 to which thickness of said 1st layer in said buffer layer is characterized by the thickness of 0.5nm - 50nm and said 2nd layer being 0.5nm - 200nm, 2, or given in three.
[Claim 7] The principal plane of the side by which said buffer layer of said substrate is arranged is a semiconductor device according to claim 1 characterized by being the field to which it leans in -4 to +4 times from the field or (111) the field just (111) in field bearing of the crystal shown with Miller indices.
[Claim 8] Said nitride system compound semiconductor layer is a semiconductor device according to claim 1 characterized by being chosen from a GaN (gallium nitride) layer, an AlInN (indium nitride aluminum) layer, an AlGaN (gallium nitride aluminum) layer, an InGaN (gallium nitride indium) layer, and an AlInGaN (gallium nitride indium aluminum) layer.

[Claim 9] It is the semiconductor device according to claim 1 which said semiconductor region consists of two or more semi-conductor layers for forming a field-effect transistor, said 1st main electrode is a source electrode, and said 2nd main electrode is a drain electrode, and is characterized by said control electrode being a gate electrode.
[Claim 10] Said semiconductor region is a semiconductor device according to claim 1 characterized by consisting of two or more semi-conductor layers for forming a high electron mobility transistor (HEMT).
[Claim 11] Said semiconductor region is a semiconductor device according to claim 1 characterized by consisting of two or more semi-conductor layers for forming a metal semiconductor field-effect transistor (MESFET).
[Claim 12] the process which prepares the substrate which is the manufacture approach of a semiconductor device of having a nitride system compound semiconductor, and consists of silicon or a silicon compound, and said substrate top -- vapor growth -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

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$x+y\leqq 1$

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula At least one sort of elements with which said M was chosen from In (indium) and B (boron) AlaMbGa1-a-bN and here,

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the manufacture approach of the semiconductor device characterized by to have the process which forms the numeric value to satisfy and the 2nd layer which comes out and consists of the ingredient shown one by one, and obtains a buffer layer, the process which form the semiconductor region for semiconductor devices which consists of at least one nitride system compound semiconductor layer by vapor growth on said buffer layer, and the process which form the 1st and 2nd main electrodes and control electrodes on the front face of said semiconductor region for semiconductor devices.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a semiconductor device and its manufacture approaches, such as MESFET which used the nitride system compound semiconductor, and HEMT.
[0002]
[Description of the Prior Art] Semiconductor devices, the metal semiconductor field-effect transistor (High Electron Mobility Transistor), i.e., MESFET (Metal Semiconductor Filed Effect Transistor) and a high electron mobility transistor, i.e., HEMT etc., using a gallium nitride system compound semiconductor etc., are well-known. in the semiconductor device using the conventional typical gallium nitride system compound semiconductor, it consists of about 500-600-degree C GaN or AlN comparatively formed at low-temperature substrate temperature on the insulating substrate which consists of sapphire -- it minds a low-temperature buffer layer (only henceforth a low-temperature buffer layer), and a compound semiconductor is formed.
[0003] That is, in forming MESFET, it forms on the insulating substrate which consists of sapphire, the layer of operation, i.e., the channel layer, which consists of the n form GaN layer which doped Si through the low-temperature buffer layer which consists of GaN or AlN, and forms a source electrode, a drain electrode, and a gate electrode in the front face of a layer of operation. Moreover, in forming HEMT, on the insulating substrate which consists of sapphire, the laminating of the electronic supply layer, the electronic transit layer, i.e., the channel layer, which consists of non-doping GaN through the low-temperature buffer layer which consists of GaN or AlN, which consists of the n form AlGaN is carried out, it is formed, and it forms a source electrode, a drain electrode, and a gate electrode in the front face of an electronic supply layer.
[0004]
[Problem(s) to be Solved by the Invention] By the way, this kind of a gallium nitride system or a nitride system semiconductor device cuts down the wafer which many components made as everyone knows and was full according to dicing, scribing, a cleavage (cleavage), etc., and is formed. Since the insulating substrate which consists of sapphire at this time had the high degree of hardness, it was difficult to perform this dicing etc. with sufficient productivity. Moreover, since sapphire was expensive, the cost of a semiconductor device became high. Moreover, when carrying out crystal growth of the nitride system compound semiconductor on silicon on sapphire, in order to obtain a flat nitride system compound semiconductor layer, it is necessary to form a low-temperature buffer layer as mentioned above. If crystal growth of the nitride system compound semiconductor layer is carried out at an elevated temperature through a low-temperature buffer layer, the comparatively flat nitride system compound semiconductor film can be formed on silicon on sapphire. However, at low temperature, when the low-temperature buffer layer which consists of GaN or AlN is formed, since the ammonia used as a nitrogen source hardly disassembles, a low-temperature buffer layer becomes an amorphous layer containing metal-like Ga and aluminum. Since crystal growth of a channel layer, i.e., the layer of operation etc., is carried out on the buffer layer of this amorphous condition, in the field near a low-temperature buffer layer, the consistency of a crystal defect becomes very high. Since the high field of this defect density functions as an n type semiconductor layer of low resistance, when operating a device, a current leaks it also to this n type semiconductor layer in addition to a layer (channel layer) of operation. Consequently, a good pinch-off property is no longer acquired. As an approach of solving this problem, the AlGaN layer is made to intervene between a buffer layer and a channel layer, and the technique of controlling current leak in a low resistance n type semiconductor

layer is proposed by JP,2000-299325,A. However, in order that mediation of an AlGaN layer may generate distortion which originated in the epitaxial layer at the stacking fault, it reduces the electron mobility of a channel layer and invites the problem of making a channel layer generate a crack further etc. For this reason, it was difficult to restrain Al amount and thickness of an AlGaN layer and to fully control leakage current as a result.

[0005] Moreover, the heat conductivity of silicon on sapphire could not fully emit the heat generated working [a device] since it is small, 0.126 W/cm-K and, but caused the fall of many properties of a transistor, such as reducing pressure-proofing, gain, etc. of a device. Furthermore, although the hetero structure which carried out the laminating of the AlGaN is generally adopted on the GaN layer by the GaN system HEMT, when growing up AlGaN on a GaN layer, a stacking fault pulls to the field inboard in AlGaN, and distortion is generated. For this stress, piezo polarization electric field occur in an interface, and if it combines with spontaneous polarization, the electric field of several MV/cm will occur in a hetero interface. Into a channel, it is accumulated by this electric field, the two-dimensional electron gas EG, i.e., 2D, of 1013cm-2 order, the fall of channel sheet resistance is achieved, and a drain current can be made to increase. This is the advantage of the GaN system HEMT which adopted the hetero structure which carried out the laminating of the AlGaN on the GaN layer.

[0006] however, silicon on sapphire -- since a coefficient of thermal expansion is larger than a nitride system compound semiconductor -- heat -- therefore, an epitaxial layer is made to generate a compressive strain irregularly Since this compressive strain works in the direction which cancels the hauling distortion in AlGaN resulting from a stacking fault, it will decrease piezo polarization electric field. For this reason, the concentration of electrons of 2D EG also falls and the engine performance of the AlGaN/GaN system HEMT cannot fully be demonstrated.

[0007] Then, the purpose of this invention is to offer a semiconductor device and its manufacture approaches, such as MESFET using the nitride system compound semiconductor which can solve an above-mentioned trouble, and HEMT.

[0008]

[Means for Solving the Problem] This invention for solving the above-mentioned technical problem and attaining the above-mentioned purpose The substrate which is the semiconductor device which has a nitride system compound semiconductor, and consists of silicon or a silicon compound, The semiconductor region for semiconductor devices containing at least one nitride system compound semiconductor layer which has been arranged on one principal plane of said substrate, and has been arranged on a buffer layer and said buffer layer, the 1st main electrode, 2nd main electrode, and control electrode which have been arranged on the front face of said semiconductor region for semiconductor devices -- having -- said buffer layer -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which it is here and said M was chosen from In (indium) and B (boron),

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$x+y\leqq 1$

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula AlaMbGa1-a-bN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

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$a+b\leqq 1$

the numeric value to satisfy and the semiconductor device characterized by consisting of a compound layer with the 2nd layer which comes out and consists of the ingredient shown are started.

[0009] In addition, as shown in claim 2, said 1st layer can be set to AlxGa1-xN, and said 2nd layer can be set to AlaGa1-aN. Moreover, as shown in claim 3, said 1st layer can be made into AlxInyGa1-x-yN, said 2nd layer can be made into AlaInbGa1-a-bN, and In (indium) can be included at least in one side of said 1st and 2nd layers. Moreover, as shown in claim 4, said 1st layer can be made into AlxByGa1-x-yN, said 2nd layer can be made into AlaBbGa1-a-bN, and B (boron) can be included at least in one side of said 1st and 2nd layers. Moreover, as shown in claim 5, as for said buffer layer, it is desirable to consist of said two or more 1st and 2nd layers, and to carry out the laminating of said the 1st layer and said 2nd layer by turns. Moreover, as shown in claim 6, it is desirable for the thickness of said 1st layer in said buffer layer to be [for the thickness of 0.5nm - 50nm and said 2nd layer] 0.5nm - 200nm. As shown in

claim 7, as for the principal plane of the side by which said buffer layer of said substrate is arranged, it is desirable that it is the field to which it leans in -4 to +4 times from the field or (111) the field just (111) in field bearing of the crystal shown with Miller indices. Moreover, as shown in claim 8, as for said nitride system compound semiconductor layer, it is desirable to be chosen from a GaN (gallium nitride) layer, an AlInN (indium nitride aluminum) layer, an AlGaN (gallium nitride aluminum) layer, an InGaN (gallium nitride indium) layer, and an AlInGaN (gallium nitride indium aluminum) layer. Moreover, as shown in claim 9, said semiconductor region can be used as two or more semi-conductor layers for forming a field-effect transistor, said 1st main electrode can be used as a source electrode, said 2nd main electrode can be used as a drain electrode, and said control electrode can be used as a gate electrode. Moreover, as shown in claim 10, said semiconductor region can be used as two or more semi-conductor layers for forming a high electron mobility transistor (HEMT). Moreover, as shown in claim 11, said semiconductor region can be used as two or more semi-conductor layers for forming a metal semiconductor field-effect transistor (MESFET). moreover, the process which prepares the substrate which consists of silicon or a silicon compound in the manufacture approach of a semiconductor device of having a nitride system compound semiconductor as shown in claim 12 and said substrate top -- vapor growth -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which said M was chosen

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from In (indium) and B (boron) here,

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula At least one sort of elements with which said M was chosen from In (indium) and B (boron) AlaMbGa1-a-bN and here,

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$a+b\leqq 1$

it is desirable to have the process which forms the numeric value to satisfy and the 2nd layer which comes out and consists of the ingredient shown one by one, and obtains a buffer layer, the process which forms the semiconductor region for semiconductor devices which consists of at least one nitride system compound semiconductor layer by vapor growth on said buffer layer, and the process which forms the 1st and 2nd main electrodes and control electrodes on the front face of said semiconductor region for semiconductor devices.

[0010]

[Effect of the Invention] According to invention of each claim, the following effectiveness is acquired.

(1) Since the substrate with which it is low cost and workability also consists of good silicon or a good silicon compound is used, reduction of ingredient cost and a production cost is possible. For this reason, the cost reduction of a semiconductor device is possible.

(2) The buffer layer to which the lattice constant formed in one principal plane of a substrate changes from the 1st layer 8 which has a value between silicon and GaN, and the 2nd layer can succeed the crystal orientation of a substrate good. Consequently, crystal orientation can be arranged and a nitride system semiconductor region can be formed in one principal plane of a buffer layer good. For this reason, the surface smoothness of a semiconductor region becomes good and the electrical characteristics of a semiconductor device also become good. When a buffer layer is formed in one principal plane of the substrate which consists of silicon at low temperature only with a GaN semi-conductor, since the difference of a lattice constant is large, silicon and GaN cannot form the nitride system semiconductor region excellent in surface smoothness in the top face of this buffer layer.

(3) As compared with the low-temperature buffer layer which consists of conventional GaN and a monolayer of AlN, crystal growth of the buffer layer which consists of the compound layer of the 1st layer 8 and the 2nd layer 9 can be carried out at an elevated temperature. For this reason, the ammonia used as a nitrogen source can be made to disassemble good, and a buffer layer does not turn into an amorphous layer. For this reason, the consistency of the crystal defect of the epitaxial growth phase, i.e., a semiconductor region, formed on a buffer layer can be made small enough, and generating of leakage current can be prevented.

(4) Since a substrate is formed from the silicon or the silicon compound which is excellent in the heat conductivity as compared with sapphire, the heat generated working [a device] can be made to radiate heat good through a substrate,

and many properties, such as pressure-proofing of a device and gain, are acquired good. The indium is contained in one [at least] layer of the 1st layer and the 2nd layer which constitute a buffer layer in invention of claim 3. The stress relaxation effectiveness between the nitride system compound semiconductor (indium nitride system compound semiconductor) containing an indium, then a substrate and a nitride system semiconductor region is acquired still better at least in one side of the 1st and 2nd layers. That is, as compared with other nitride system compound semiconductors which do not contain In as a configuration element, for example, GaN, AlN, etc., the substrate and coefficient of thermal expansion which consist of silicon or a silicon compound approximate more the indium nitride system compound semiconductor which constitutes at least one side of the 1st and 2nd layers, for example, InN, InGaN, AlInN, AlInGaN, etc. For this reason, distortion of the semiconductor region resulting from the difference of the coefficient of thermal expansion between a substrate and a nitride system semiconductor region can be prevented good by including an indium in one [at least] layer among the 1st layer and the 2nd layer which constitute a buffer layer. B (boron) is contained in one [at least] layer of the 1st layer and the 2nd layer which constitute a buffer layer in invention of claim 4. The buffer layer containing B (boron) has a coefficient of thermal expansion near the coefficien of thermal expansion of the substrate which consists of silicon or a silicon compound rather than the buffer layer which does not have B (boron) **. For this reason, according to the buffer layer containing B (boron), distortion of the nitride system semiconductor region resulting from the coefficient-of-thermal-expansion difference between the substrates and nitride system semiconductor regions which consist of silicon or a silicon compound can be prevented good. In invention of claim 5, since the laminating of two or more 1st layers and two or more 2nd layers is carried out by turns and a buffer layer is constituted, two or more 1st thin layers are distributed. Consequently, buffer ability good as the whole buffer layer can be obtained, and the crystallinity of the semiconductor region formed on a buffer layer becomes good. According to invention of claim 6, the buffer ability of a buffer layer can improve and surface smoothness of a nitride system semiconductor region can be improved. According to invention of claim 7, a buffer layer and a semiconductor region can be formed good on a substrate. namely, the thing abolished for the atomic step on the front face of a crystal of a buffer layer and a semiconductor region, i.e., the step in atomic level, by making field bearing of the principal plane of a substrate into a field or (111) the field from a field where an OFF include angle is small just (111) -- or it can lessen. If a buffer layer and a semiconductor region are formed on a principal plane with the large off include angle from a field just (111), it will see on atomic level to this etc., and a comparatively large step will arise. Although some steps do not become a problem so much when an epitaxial growth phase is comparatively thick, in the case of the semiconductor device which has the film of thickness, there is a possibility of causing the fall of a property. On the other hand, a field or the field where an off include angle is small, then a step become small just (111) about the principal plane of a substrate, and a buffer layer and a semiconductor region are formed good. According to invention of claim 12, a semiconductor device with a sufficient property can be formed cheaply and easily.

[0011]

[The 1st operation gestalt] Next, HEMT using the gallium nitride system compound semiconductor applied to the 1st operation gestalt of this invention with reference to drawing 1 - drawing 3 is explained.

[0012] HEMT concerning the 1st operation gestalt of this invention shown in drawing 1 consists of a buffer layer, the substrate 1, i.e., the substrate, which consists of silicon, 2, the semiconductor region 3 for HEMT elements, the source electrode 4 as the 1st electrode, the drain electrode 5 as the 2nd electrode, the gate electrode 6 as a control electrode, and an insulator layer 7.

[0013] The HEMT element semiconductor region 3 has the electronic transit layer 10 which consists of impurity non-doping GaN, the spacer layer 11 which consists of non-doping aluminum0.2Ga0.8N, and the electronic supply layer 12 which consists of n form aluminum0.2Ga0.8N by which Si is doped as an n form impurity. Each class 10, 11, and 12 of the semiconductor region 3 for components consists of the gallium nitride system compound semiconductor which used nitrogen and a gallium as the base. The electronic transit layer 10 arranged on a buffer layer 2 can also be called a channel layer, and has the thickness of 500nm. It controls that the spacer layer 11 arranged on the electronic transit layer 10 has the thickness of 7nm, and the silicon as an n form impurity of the electronic supply layer 12 diffuses it in the electronic transit layer 10. The electronic supply layer 12 arranged on the spacer layer 11 can also be called a barrier layer, a layer of operation, or a channel layer, and has the thickness of 10nm. The source electrode 4 and the drain electrode 5 carry out ohmic contact at the electronic supply layer 12, and are carrying out Schottky contact of the gate electrode 6 to the electronic supply layer 12. In addition, the high contact layer of n form high impurity concentration can be prepared between the source electrode 4 and the drain electrode 5, and the electronic supply layer

12. The insulator layer 7 which consists of SiO2 has covered the front face of a semiconductor region 10.
[0014] the electronic supply layer 12 and the spacer layer 11 -- **** -- since it is the thin film, it functions on a longitudinal direction as an insulating material, and functions on a lengthwise direction as a conductor. Therefore, at the time of actuation of HEMT, an electron flows in the path of the source electrode 4, the electronic supply layer 12, the spacer layer 11, the electronic transit layer 10, the spacer layer 11, the electronic supply layer 12, and the drain electrode 5. The flow of this electron, i.e., the flow of a current, is adjusted with the control voltage impressed to the gate electrode 6.
[0015] A substrate 1 consists of p form silicon single crystal which contains 3 group elements, such as B (boron), as an electric conduction form decision impurity. Principal plane 1a of the side by which the buffer layer 2 of this substrate 1 is arranged is a field just (111) in field bearing of the crystal shown with Miller indices. The high impurity concentration of this substrate 1 is a comparatively low value (about [for example, / 1x1013cm - three to 1x1016cm -] 3) in order to reduce the leakage current which passes along a substrate 1, and the resistivity of this substrate 1 is a comparatively high value, for example, 1.0 ohm-cm - 500 ohm-cm extent. A substrate 1 has the comparatively thick thickness of about 350 micrometers, and functions as a base material of a semiconductor region 3 and a buffer layer 2.
[0016] The buffer layer 2 arranged so that one whole principal plane of a substrate 1 may be covered consists of the compound layer to which the laminating of two or more 1st layers 8 and two or more 2nd layers 9 was carried out by turns. In drawing 1 , on account of illustration, although a part of buffer layer 2 is shown, a buffer layer 2 has the 1st 20 layer 8 and the 2nd 20 layer 9 in fact.
[0017] the 1st layer 8 -- chemical formula AlxGa1-xN -- it is here, and it comes out and x is formed with the numeric value of the arbitration which satisfies 0< x<=1, and the ingredient which can be shown. That is, the 1st layer 8 is formed by AlN (alumimium nitride) or AlGaN (gallium nitride aluminum). With drawing 1 and the operation gestalt of drawing 2 , AlN (alumimium nitride) by which x of said formula is equivalent to the ingredient set to 1 is used for the 1st layer 8. The 1st layer 8 is very thin film which has insulation. The 1st lattice constant and coefficient of thermal expansion of a layer 8 are closer to a silicon substrate 1 than the 2nd layer 9.
[0018] the 2nd layer 9 -- GaN (gallium nitride) or chemical formula AlyGa1-yN -- **** to which it is here, and it appears and y changes from y<x, the numeric value of arbitration with which are satisfied of 0< y<1, and the ingredient which can be shown -- it is the thin film. When using the semi-conductor which does not contain the electric conduction form decision impurity which consists of AlyGa1-yN as the 2nd layer 9, in order to prevent a crack with a possibility of generating according to increase of aluminum (aluminum), it is desirable to make y for it to be larger than the value, 0 [i.e.,], with which are satisfied of 0< y<0.8, and smaller than 0.8. In addition, the 2nd layer 9 of this 1st operation gestalt consists of GaN equivalent to y= 0 in the above-mentioned chemical formula. said 2nd layer -- chemical formula AlyGa1-yN -- the numeric value with which y is satisfied of y<x and 0<=y<1 here -- it can also come out and express.
[0019] The desirable thickness of the 1st layer 8 of a buffer layer 2 is 0.5nm - 50nm, i.e., 5-500A. When the thickness of the 1st layer 8 is less than 0.5nm, it becomes impossible to keep good the surface smoothness of the semiconductor region 3 for components formed in the top face of a buffer layer 2. When the thickness of the 1st layer 8 exceeds 50nm, a possibility that a crack may occur is in the 1st layer 8 by hauling distortion which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8.
[0020] The desirable thickness of the 2nd layer 9 is 0.5nm - 200nm, i.e., 5-2000A. When the thickness of the 2nd layer 9 is less than 0.5nm, it becomes difficult to grow up evenly the semiconductor region 3 for components which grows on the 1st layer 8 and a buffer layer 2. Moreover, if the thickness of the 2nd layer 9 exceeds 200nm, with the compressive stress which originates in the stacking fault of the 2nd layer 9 and the 1st layer 8, and is generated in the 2nd layer 9, the electron density of the channel layer 10 will fall and the property of HEMT will deteriorate. Furthermore, it is good preferably to make thickness of the 2nd layer 9 larger than the thickness of the 1st layer 8. If it does in this way, in holding down the distorted magnitude which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8 to extent which a crack does not generate in the 1st layer 9, and maintaining at the concentration-of-electrons high concentration of the channel layer 10, it will become advantageous.
[0021] Next, the manufacture approach of a semi-conductor semiconductor device that the 1st layer 8 was set to AlN and the 2nd layer 9 was set to GaN is explained.

[0022] First, the substrate 1 which consists of p form silicon semi-conductor with which p form impurity shown in (A) of drawing 3 was introduced is prepared. One principal plane 1a of the silicon substrate 1 for forming a buffer layer 2 is a field, i.e., an exact (111) field, just (111) in field bearing of the crystal shown with Miller indices. However, principal plane 1a of a substrate 1 can be made to incline in the range which is shown by 0 in drawing 3 (111) and which is just shown by -theta - +theta to a field. - The range of theta - +theta is -4 degrees - +4 degrees, is -3 degrees - +3 degrees preferably, and is -2 degrees - +2 degrees more preferably. losing the step in the atomic level at the time of carrying out epitaxial growth of a buffer layer 2 and the semiconductor region 3 for components by making just (111) crystal orientation of principal plane 1a of a silicon substrate 1 into a field or (111) the field from a field where an OFF include angle is small -- or it can be made small.
[0023] Next, as shown in drawing 3 (B), the buffer layer 2 on principal plane 1a of a substrate 1 is formed by repeating and carrying out the laminating of the 1st layer 8 which consists of AlN, and the 2nd layer 9 which consists of GaN, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of p form silicon single crystal pretreated by HF system etchant is arranged in the reaction chamber of an MOCVD system, first, thermal annealing for about 10 minutes is performed at 950 degrees C, and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas and NH3 (ammonia) gas are supplied for about 65 seconds in a reaction chamber, and the 1st layer 8 which changes from an AlN layer with a thickness of about 10nm to one principal plane of a substrate 1 is formed. After making whenever [stoving temperature / of a substrate 1] into 1120 degrees C in this example, it is about 63micromol/min and NH3 in the flow rate of TMA gas, i.e., the amount of supply of aluminum. Flow rate 3 of gas, i.e., NH, The amount of supply was made into about 0.14 mol/min. Then, after making whenever [stoving temperature / of a substrate 1] into 1120 degrees C and stopping supply of TMA gas, it is TMG (trimethylgallium) gas and NH3 in a reaction chamber. Gas (ammonia) is supplied for about 90 seconds, and the 2nd layer 9 which consists of GaN of n form with a thickness of about 30nm is formed in the top face of the 1st layer 8 which consists of the above AlN formed in one principal plane of a substrate 1. At this example, it is about 60micromol/min and NH3 in the flow rate of TMG gas, i.e., the amount of supply of Ga. Flow rate 3 of gas, i.e., NH, The amount of supply was made into about 0.14 mol/min. In this example, 40 layers obtain the buffer layer 2 by which the laminating was carried out in the sum total of the 1st layer 8 which repeats formation of the 1st layer 8 which consists of above-mentioned AlN, and the 2nd layer 9 which consists of GaN 20 times, and consists of AlN, and the 2nd layer 9 which consists of GaN. The 1st layer 8 which consists of AlN, of course, and the 2nd layer 9 which consists of GaN are also changeable into the number of arbitration, such as 50 etc. layers, respectively.
[0024] next, MOCVD of common knowledge on the top face of a buffer layer 2 -- the form semiconductor region 3 for HEMT elements is formed by law. That is, the substrate 1 with which the buffer layer 2 was formed in the top face is arranged in the reaction chamber of an MOCVD system, and they are trimethylgallium gas, i.e., TMG gas, and NH3 first in a reaction chamber. The electronic transit layer 10 which consists of GaN which supplies gas (ammonia) for 15 minutes and does not include un-doping [with a thickness of about 500nm / GaN], i.e., an electric conduction form decision impurity, on the top face of a buffer layer 2 is formed. At this example, it is about 62micromol/min and NH3 in the flow rate of TMG gas, i.e., the amount of supply of Ga. Flow rate 3 of gas, i.e., NH, About 0.23 mols of amount of supply were set to /min.
[0025] Next, the spacer layer 11 which consists of aluminum0.2Ga0.8N which supplies TMG gas and ammonia gas to the TMA gas in a reaction chamber for 85 seconds, and does not include un-doping, i.e., an electric conduction form decision impurity, on the top face of the electronic transit layer 10 is formed in the thickness of 7nm. In this example, about 0.23 mols of flow rates of about 15micromol / min, and NH3 gas were set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to /min for the flow rate of about 8.4micromol/min and TMG gas.
[0026] Next, after interrupting crystal growth for about 15 seconds, the electronic supply layer 12 which supplies TMA gas, TMG gas, ammonia gas, and SiH4 (silane) gas for about 98 seconds in a reaction chamber, and changes from aluminum0.2Ga0.8N to the top face of the spacer layer 11 is formed in the thickness of about 10nm. In this example, about 0.23 mols of flow rates of /min and SiH4 gas were set [the flow rate of the TMA gas at this time / the flow rate of about 8.4micromol/min and TMG gas] to about 21 nmol(s) / min for the flow rate of about 15micromol / min, and ammonia gas.
[0027] Then, the silicon substrate 1 in which the semiconductor region 3 and the buffer layer 2 were formed is taken out from an MOCVD system, and the insulator layer 7 which consists of silicon oxide all over a semiconductor region 3 by well-known plasma CVD is formed. Thickness of an insulator layer 7 is set to about 100nm.

[0028] Although one HEMT is shown in drawing 1 , much HEMT(s) are made to coincidence using one semi-conductor wafer 1, i.e., substrate, at the time of this manufacture. For this reason, with photolithography, a semiconductor region 3 and the component isolation region of a buffer layer 2 are etched to a silicon substrate 1 by reactive ion etching using the mixed gas of 3 boron chloride (BCI3) and hydrogen, and isolation of HEMT is performed. Thus, if isolation is carried out, the electrical characteristics of each component field etc. can be inspected good, without being influenced of other components.
[0029] Next, after using photolithography and fluoric acid system etchant and forming opening for a source electrode and drain electrode formation in an insulator layer 7, using electron beam evaporation etc., laminating formation is carried out one by one, lift off of Ti (titanium) and the aluminum (aluminum) is carried out, and the source electrode 4 and the drain electrode 5 are formed. Also when forming a gate electrode, opening is formed in an insulator layer 7 in the same procedure, and the gate electrode 6 which vapor-deposits and carries out lift off of Pd (palladium), Ti (titanium), and the Au(gold) by electron beam evaporation, and has a function as a shot key barrier electrode is formed. Then, the semiconductor device (HEMT chip) which carried out cutting separation of the epitaxial wafer in the component isolation region, and turned the individual exception according to the well-known dicing process etc. is completed.
[0030] According to HEMT of this operation gestalt, the following effectiveness is acquired.
(1) Since the substrate 1 with which it is low cost and workability also consists of good silicon is used, reduction of ingredient cost and a production cost is possible. For this reason, the cost reduction of HEMT is possible.
(2) The buffer layer 2 which consists of the 1st layer 8 to which the lattice constant formed in one principal plane of a substrate 1 changes from AlN which has a value between silicon and GaN, and the 2nd layer 9 can succeed the crystal orientation of the substrate 1 which consists of silicon good. Consequently, crystal orientation can be arranged and the GaN system semiconductor region 3 can be formed in one principal plane of a buffer layer 2 good. For this reason, the surface smoothness of a semiconductor region 3 becomes good, and the electrical characteristics of HEMT also become good. When a buffer layer is formed in one principal plane of the substrate 1 which consists of silicon at low temperature only with a GaN semi-conductor, since the difference of a lattice constant is large, silicon and GaN cannot form the GaN system semiconductor region excellent in surface smoothness in the top face of this buffer layer.
(3) As compared with the low-temperature buffer layer which consists of conventional GaN and a monolayer of AlN, crystal growth of the buffer layer 2 which consists of the compound layer of the 1st layer 8 which consists of AlN, and the 2nd layer 9 which consists of GaN can be carried out at an elevated temperature. For this reason, the ammonia used as a nitrogen source can be made to disassemble good, and a buffer layer 2 does not turn into an amorphous layer. For this reason, the consistency of the crystal defect of the epitaxial growth phase 3, i.e., a semiconductor region, formed on a buffer layer 2 can be made small enough, and generating of leakage current can be prevented. Consequently, HEMT with a good pinch-off property can be offered.
(4) Since a substrate 1 is formed from the silicon which is excellent in the heat conductivity as compared with sapphire, the heat generated working [a device] can be made to radiate heat good through a substrate 1, and many properties, such as pressure-proofing of a device and gain, are acquired good.
(5) a silicon substrate 1 -- a nitride system compound semiconductor -- comparing -- since a coefficient of thermal expansion is small -- heat -- it originated irregularly -- pull and distortion joins an epitaxial layer. For this reason, the tensile stress of the interface of AlGaN/GaN between the tooth-space layer 11 and the electronic transit layer 10 can be strengthened further, and the piezo electric field effect can be heightened as a result. For this reason, electron density of the electronic transit layer 10, i.e., a channel, can be made into high concentration as compared with HEMT which used silicon on sapphire, and it becomes possible to decrease the sheet resistance of the electronic transit layer 10, i.e., a channel, and to increase a drain current.
[0031]
[The 2nd operation gestalt] Next, MESFET of the 2nd operation gestalt is explained with reference to drawing 4 . However, in drawing 4 , the same sign is substantially given to the same part with drawing 1 R> 1, and the explanation is omitted. MESFET of drawing 4 prepares n type semiconductor field 3a which consists the semiconductor region 3 of HEMT of drawing 1 of the GaN compound semiconductor layer by which Si was doped as an n form impurity, and forms others identically to drawing 1 . That is, in MESFET of drawing 4 , a silicon substrate 1, a buffer layer 2, the source electrode 4, the drain electrode 5, the gate electrode 6, and the insulator layer 7 are formed like what is shown with the same sign by drawing 1 . N type semiconductor field 3a can also be called a channel layer or a barrier layer,

and is arranged on the buffer layer 2. The source electrode 4 and the gate electrode 5 carry out ohmic contact at n type semiconductor field 3a, and are carrying out shot key barrier contact of the gate electrode 6 at n type semiconductor field 3a.

[0032] The manufacture approaches other than GaN semiconductor region 3a of MESFET of drawing 4 are the same as that of the 1st operation gestalt. When forming GaN semiconductor region 3a, TMG gas, NH3 gas, and SiH4 (silane) gas are supplied for about 450 seconds in the reaction chamber used at the time of formation of a buffer layer 2, and with a thickness of about 150nm n type semiconductor field 3a is formed in the top face of the buffer layer 2 formed in one principal plane of a substrate 1. In this example, the flow rate of 0.23 mol/min and SiH4 gas, i.e., the amount of supply of Si, was made [the flow rate of TMG gas, i.e., the amount of supply of Ga] into 21 nmol/min for the flow rate of about 60micromol/min and NH3 gas, i.e., the amount of supply of NH3.

[0033] MESFET of drawing 4 has the same effectiveness as (1) stated in the column of explanation of the effectiveness of HEMT of drawing 1 , (2), (3), and (4). That is, it becomes possible to improve the surface smoothness of making a substrate 1 cheap and semiconductor region 3a, and crystallinity, to improve the property of MESFET, and to radiate the heat of semiconductor region 3a good through a silicon substrate 1.

[0034]

[The 3rd operation gestalt] The configuration of the buffer layer 2 of the 1st and 2nd operation gestalten is changeable. Drawing 5 shows a part of buffer layer 2a which follows the 3rd usable operation gestalt at HEMT, MESFET, etc. Buffer layer 2a of this drawing 5 consists of what carried out the laminating of the 2nd layer 9a of two or more 1st layer 8a and plurality by turns. 1st layer 8a -- chemical formula AlxInyGa1-x-yN -- it is here, and it comes out and x and y are formed with the numeric value of the arbitration which satisfies 0< x<=1, 0<=y<1, and x+y<=1, and the ingredient which can be shown. That is, 1st layer 8a was chosen from AlN (alumimium nitride), AlGaN (gallium nitride aluminum), AlInN (indium nitride aluminum), and AlGaInN (gallium nitride indium aluminum), and is formed. With the operation gestalt of drawing 5 , aluminum0.5In0.01Ga0.49N equivalent to the ingredient with which x of said formula was set to 0.5, and y was set to 0.01 is used for 1st layer 8a. **** in which 1st layer 8a has insulation -- it is the thin film. The 1st lattice constant and coefficient of thermal expansion containing aluminum of layer 8a have a value between the lattice constant of a silicon substrate 1 and a coefficient of thermal expansion, the lattice constant of semiconductor region 3a, and a coefficient of thermal expansion.

[0035] 2nd layer 9a -- chemical formula AlaInbGa1-a-bN -- it is here and a and b are the numeric value of the arbitration which satisfies 0<=a<1, 0<=b<1, and a+b<=1, and the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9a was chosen from GaN, AlN, InN, InGaN, AlGaN, AlInN, and AlInGaN, and is formed. With the operation gestalt of drawing 5 , aluminum0.05In0.35Ga0.6N equivalent to the ingredient with which a of said formula was set to 0.05, and b was set to 0.35 is used for 2nd layer 9a. It is larger than the band gap of 1st layer 8a, the gap, i.e., the band gap, between the valence band of 2nd layer 9a, and a conduction band.

[0036] Next, 1st layer 8a explains the manufacture approach of buffer layer 2a that aluminum0.5In0.01Ga0.49N and 2nd layer 9a were set to aluminum0.05In0.35Ga0.6N. Buffer layer 2a is formed on principal plane 1a of the same substrate 1 as the 1st operation gestalt. This buffer layer 2a is formed by repeating and carrying out the laminating of 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, and the 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, TMIn (trimethylindium) gas, and NH3 (ammonia) gas are supplied for about 24 seconds in a reaction chamber, and 1st layer 8a which changes from aluminum0.5In0.01Ga0.49N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 1 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 800 degrees C, the flow rate of 47micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas, i.e., the amount of supply of aluminum, / the flow rate of about 14micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 31micromol/min and TMIn gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas, TMG gas, and TMIn gas to 750 degrees C, TMA gas, TMG gas, TMIn gas, and NH3 (ammonia) gas are supplied for about 83 seconds after an appropriate time, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N whose thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8a. In

addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 59micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas / the flow rate of 2.8micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 46micromol/min and TMIn gas. In this example, 1st layer 8a which repeats formation of 1st layer 8a which consists of above-mentioned aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N 10 times, and consists of aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N form the buffer layer 2 by which the 20-layer laminating was carried out by turns. The 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, of course, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N are also changeable into the number of arbitration, such as 50 etc. layers, respectively.

[0037] Since buffer layer 2a of the 3rd operation gestalt of drawing 5 has the same effectiveness as the 1st operation gestalt of drawing 1 and the indium is further contained in buffer layer 2a, it has the effectiveness of the ability to make the coefficient of thermal expansion of buffer layer 2a approximate to a silicon substrate 1 rather than the case where an indium is not included in buffer layer 2a.

[0038]

[The 4th operation gestalt] Buffer layer 2b of the 4th operation gestalt shown in drawing 6 transforms the buffer layer 2 of drawing 1 and drawing 4 , and consists of the crosswise lamination object of the 1st and 2nd layers 8b and 9b. 1st layer 8b -- chemical formula AlxByGa1-x-yN -- it is here, and it comes out and x and y are formed with the numeric value of the arbitration which satisfies 0< x<=1, 0<=y<1, and x+y<=1, and the ingredient which can be shown. That is, 1st layer 8b was chosen from AlN (alumimium nitride), AlGaN (gallium nitride aluminum), AlBN (boron nitride aluminum), and AlBGaN (gallium nitride boron aluminum), and is formed. With the operation gestalt of drawing 6 , aluminum0.5Ga0.5N equivalent to the ingredient with which x of said formula was set to 0.5, and y was set to 0 is used for 1st layer 8b. 1st layer 8b is very thin film which has insulation. The 1st lattice constant and coefficient of thermal expansion of layer 8b are closer to a silicon substrate 1 than 2nd layer 9b.

[0039] 2nd layer 9b -- chemical formula AlaBbGa1-a-bN -- it is here and a and b are the numeric value of the arbitration which satisfies 0<=a<1, 0<=b<1, and a+b<=1, and the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9b is a layer containing at least one element chosen from aluminum, B, and Ga, and N, for example, was chosen from GaN, BN, AlN, BGaN, AlGaN, AlBN, and AlBGaN, and is formed. With the operation gestalt of drawing 6 , B0.3Ga0.7N equivalent to the ingredient with which a of said formula was set to 0 and b was set to 0.3 is used for 2nd layer 9b. It is larger than the band gap of 1st layer 8b, the gap, i.e., the band gap, between the valence band of 2nd layer 9b, and a conduction band.

[0040] Buffer layer 2b is formed by repeating and carrying out the laminating of 1st layer 8b which consists of aluminum0.5Ga0.5N, and the 2nd layer 9b which consists of B0.3Ga0.7N on principal plane 1a of a substrate 1 which has a field just (111), well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, and NH3 (ammonia) gas are supplied for about 27 seconds in a reaction chamber, and 1st layer 8b which changes from aluminum0.5Ga0.5N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 11 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 1080 degrees C, the flow rate of 31micromol/min and NH3 gas, i.e., the amount of supply of NH3, was set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to about 0.14 mols / min for the flow rate of about 31micromol/min and TMG gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas to 1120 degrees C, TEB (triethyl boron) gas, TMG gas, and NH3 (ammonia) gas are supplied for about 85 seconds after an appropriate time, and 2nd layer 9b which consists of B0.3Ga0.7N of n form where thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8b. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 63micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TEB gas, i.e., the amount of supply of boron,] into about 0.14 mol/min for the flow rate of 75micromol/min and TMG gas, i.e., the amount of supply of a gallium. In this example, 1st layer 8b which repeats formation of 2nd layer 9b which consists of the 1st layer 8b and B0.3Ga0.7N which consists of above-mentioned aluminum0.5Ga0.5N 50 times, and consists of aluminum0.5Ga0.5N, and 2nd layer 9b which consists of B0.3Ga0.7N form buffer layer 2b by which the 100-layer laminating was carried out by turns in total. 1st layer 8b which consists of aluminum0.5Ga0.5N, of course,

and 2nd layer 9b which consists of B0.3Ga0.7N are also changeable into the number of arbitration, such as 25 etc. layers, respectively.
[0041] Since buffer layer 2b of drawing 6 has the same effectiveness as the buffer layer 2 of drawing 1 and boron is further contained in 2nd layer 9b, compared with the case where 2nd layer 9b does not contain boron, it becomes strong, and has the effectiveness that generating of a crack can be prevented and 2nd layer 9b can be formed comparatively thickly.
[0042]
[Modification(s)] This invention is not limited to an above-mentioned operation gestalt, and the next deformation is possible for it.
(1) A substrate 11 can be used as silicon compounds, such as polycrystalline silicon other than single crystal silicon, or SiC.
(2) The electric conduction form of each class of semiconductor regions 3 and 3a can be made into an example and reverse.
(3) Each class of semiconductor regions 3 and 3a can be used as the gallium nitride system compound semiconductor or indium nitride system compound semiconductor chosen from GaN (gallium nitride), AlInN (indium nitride aluminum), AlGaN (gallium nitride aluminum), InGaN (gallium nitride indium), and AlInGaN (gallium nitride indium aluminum).
(4) In HEMT of drawing 1 , the electronic supply layer 12 and the same electronic supply layer can be prepared between a barrier layer 10, i.e., an electronic transit layer, and a buffer layer 2.
(5) The insulated-gate mold electrical quantity effectiveness transistor can be prepared instead of HEMT and MESFET.

(6) One layer can make [more] the number of buffer layers 2 and 2a and the 1st layers 8, 8a, and 8b of 2b than the 2nd layer 9, 9a, and 9b, and buffer layers 2 and 2a and the maximum upper layer of 2b can be used as the 1st layer 8, 8a, and 8b. Moreover, the one layer of the number of the 2nd layers 9, 9a, and 9b can also be conversely made [many] rather than the number of the 1st layers 8, 8a, and 8b.
(7) The 1st Layers 8, 8a, and 8b and 2nd layer 9, 9a, and 9b may contain an impurity in the range which does not check these functions.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] This invention relates to a semiconductor device and its manufacture approaches, such as MESFET which used the nitride system compound semiconductor, and HEMT.
[0002]

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PRIOR ART

[Description of the Prior Art] Semiconductor devices, the metal semiconductor field-effect transistor (High Electron Mobility Transistor), i.e., MESFET (Metal Semiconductor Filed Effect Transistor) and a high electron mobility transistor, i.e., HEMT etc., using a gallium nitride system compound semiconductor etc., are well-known. in the semiconductor device using the conventional typical gallium nitride system compound semiconductor, it consists of about 500-600-degree C GaN or AlN comparatively formed at low-temperature substrate temperature on the insulating substrate which consists of sapphire -- it minds a low-temperature buffer layer (only henceforth a low-temperature buffer layer), and a compound semiconductor is formed.
[0003] That is, in forming MESFET, it forms on the insulating substrate which consists of sapphire, the layer of operation, i.e., the channel layer, which consists of the n form GaN layer which doped Si through the low-temperature buffer layer which consists of GaN or AlN, and forms a source electrode, a drain electrode, and a gate electrode in the front face of a layer of operation. Moreover, in forming HEMT, on the insulating substrate which consists of sapphire, the laminating of the electronic supply layer, the electronic transit layer, i.e., the channel layer, which consists of non-doping GaN through the low-temperature buffer layer which consists of GaN or AlN, which consists of the n form AlGaN is carried out, it is formed, and it forms a source electrode, a drain electrode, and a gate electrode in the front face of an electronic supply layer.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to invention of each claim, the following effectiveness is acquired.
(1) Since the substrate with which it is low cost and workability also consists of good silicon or a good silicon compound is used, reduction of ingredient cost and a production cost is possible. For this reason, the cost reduction of a semiconductor device is possible.
(2) The buffer layer to which the lattice constant formed in one principal plane of a substrate changes from the 1st layer 8 which has a value between silicon and GaN, and the 2nd layer can succeed the crystal orientation of a substrate good. Consequently, crystal orientation can be arranged and a nitride system semiconductor region can be formed in one principal plane of a buffer layer good. For this reason, the surface smoothness of a semiconductor region becomes good and the electrical characteristics of a semiconductor device also become good. When a buffer layer is formed in one principal plane of the substrate which consists of silicon at low temperature only with a GaN semi-conductor, since the difference of a lattice constant is large, silicon and GaN cannot form the nitride system semiconductor region excellent in surface smoothness in the top face of this buffer layer.
(3) As compared with the low-temperature buffer layer which consists of conventional GaN and a monolayer of AlN, crystal growth of the buffer layer which consists of the compound layer of the 1st layer 8 and the 2nd layer 9 can be carried out at an elevated temperature. For this reason, the ammonia used as a nitrogen source can be made to disassemble good, and a buffer layer does not turn into an amorphous layer. For this reason, the consistency of the crystal defect of the epitaxial growth phase, i.e., a semiconductor region, formed on a buffer layer can be made small enough, and generating of leakage current can be prevented.
(4) Since a substrate is formed from the silicon or the silicon compound which is excellent in the heat conductivity as compared with sapphire, the heat generated working [a device] can be made to radiate heat good through a substrate, and many properties, such as pressure-proofing of a device and gain, are acquired good. The indium is contained in one [at least] layer of the 1st layer and the 2nd layer which constitute a buffer layer in invention of claim 3. The stress relaxation effectiveness between the nitride system compound semiconductor (indium nitride system compound semiconductor) containing an indium, then a substrate and a nitride system semiconductor region is acquired still better at least in one side of the 1st and 2nd layers. That is, as compared with other nitride system compound semiconductors which do not contain In as a configuration element, for example, GaN, AlN, etc., the substrate and coefficient of thermal expansion which consist of silicon or a silicon compound approximate more the indium nitride system compound semiconductor which constitutes at least one side of the 1st and 2nd layers, for example, InN, InGaN, AlInN, AlInGaN, etc. For this reason, distortion of the semiconductor region resulting from the difference of the coefficient of thermal expansion between a substrate and a nitride system semiconductor region can be prevented good by including an indium in one [at least] layer among the 1st layer and the 2nd layer which constitute a buffer layer. B (boron) is contained in one [at least] layer of the 1st layer and the 2nd layer which constitute a buffer layer in invention of claim 4. The buffer layer containing B (boron) has a coefficient of thermal expansion near the coefficient of thermal expansion of the substrate which consists of silicon or a silicon compound rather than the buffer layer which does not have B (boron) **. For this reason, according to the buffer layer containing B (boron), distortion of the nitride system semiconductor region resulting from the coefficient-of-thermal-expansion difference between the substrates and nitride system semiconductor regions which consist of silicon or a silicon compound can be prevented good. In invention of claim 5, since the laminating of two or more 1st layers and two or more 2nd layers is carried out by turns and a buffer layer is constituted, two or more 1st thin layers are distributed. Consequently, buffer ability good as the

whole buffer layer can be obtained, and the crystallinity of the semiconductor region formed on a buffer layer becomes good. According to invention of claim 6, the buffer ability of a buffer layer can improve and surface smoothness of a nitride system semiconductor region can be improved. According to invention of claim 7, a buffer layer and a semiconductor region can be formed good on a substrate. namely, the thing abolished for the atomic step on the front face of a crystal of a buffer layer and a semiconductor region, i.e., the step in atomic level, by making field bearing of the principal plane of a substrate into a field or (111) the field from a field where an OFF include angle is small just (111) -- or it can lessen. If a buffer layer and a semiconductor region are formed on a principal plane with the large off include angle from a field just (111), it will see on atomic level to this etc., and a comparatively large step will arise. Although some steps do not become a problem so much when an epitaxial growth phase is comparatively thick, in the case of the semiconductor device which has the film of thickness, there is a possibility of causing the fall of a property. On the other hand, a field or the field where an off include angle is small, then a step become small just (111) about the principal plane of a substrate, and a buffer layer and a semiconductor region are formed good. According to invention of claim 12, a semiconductor device with a sufficient property can be formed cheaply and easily.

[0011]

[The 1st operation gestalt] Next, HEMT using the gallium nitride system compound semiconductor applied to the 1st operation gestalt of this invention with reference to drawing 1 - drawing 3 is explained.

[0012] HEMT concerning the 1st operation gestalt of this invention shown in drawing 1 consists of a buffer layer, the substrate 1, i.e., the substrate, which consists of silicon, 2, the semiconductor region 3 for HEMT elements, the source electrode 4 as the 1st electrode, the drain electrode 5 as the 2nd electrode, the gate electrode 6 as a control electrode, and an insulator layer 7.

[0013] The HEMT element semiconductor region 3 has the electronic transit layer 10 which consists of impurity non-doping GaN, the spacer layer 11 which consists of non-doping aluminum0.2Ga0.8N, and the electronic supply layer 12 which consists of n form aluminum0.2Ga0.8N by which Si is doped as an n form impurity. Each class 10, 11, and 12 of the semiconductor region 3 for components consists of the gallium nitride system compound semiconductor which used nitrogen and a gallium as the base. The electronic transit layer 10 arranged on a buffer layer 2 can also be called a channel layer, and has the thickness of 500nm. It controls that the spacer layer 11 arranged on the electronic transit layer 10 has the thickness of 7nm, and the silicon as an n form impurity of the electronic supply layer 12 diffuses it in the electronic transit layer 10. The electronic supply layer 12 arranged on the spacer layer 11 can also be called a barrier layer, a layer of operation, or a channel layer, and has the thickness of 10nm. The source electrode 4 and the drain electrode 5 carry out ohmic contact at the electronic supply layer 12, and are carrying out Schottky contact of the gate electrode 6 to the electronic supply layer 12. In addition, the high contact layer of n form high impurity concentration can be prepared between the source electrode 4 and the drain electrode 5, and the electronic supply layer 12. The insulator layer 7 which consists of SiO2 has covered the front face of a semiconductor region 10.

[0014] the electronic supply layer 12 and the spacer layer 11 -- **** -- since it is the thin film, it functions on a longitudinal direction as an insulating material, and functions on a lengthwise direction as a conductor. Therefore, at the time of actuation of HEMT, an electron flows in the path of the source electrode 4, the electronic supply layer 12, the spacer layer 11, the electronic transit layer 10, the spacer layer 11, the electronic supply layer 12, and the drain electrode 5. The flow of this electron, i.e., the flow of a current, is adjusted with the control voltage impressed to the gate electrode 6.

[0015] A substrate 1 consists of p form silicon single crystal which contains 3 group elements, such as B (boron), as an electric conduction form decision impurity. Principal plane 1a of the side by which the buffer layer 2 of this substrate 1 is arranged is a field just (111) in field bearing of the crystal shown with Miller indices. The high impurity concentration of this substrate 1 is a comparatively low value (about [for example, / 1x1013cm - three to 1x1016cm -] 3) in order to reduce the leakage current which passes along a substrate 1, and the resistivity of this substrate 1 is a comparatively high value, for example, 1.0 ohm-cm - 500 ohm-cm extent. A substrate 1 has the comparatively thick thickness of about 350 micrometers, and functions as a base material of a semiconductor region 3 and a buffer layer 2.

[0016] The buffer layer 2 arranged so that one whole principal plane of a substrate 1 may be covered consists of the compound layer to which the laminating of two or more 1st layers 8 and two or more 2nd layers 9 was carried out by turns. In drawing 1 , on account of illustration, although a part of buffer layer 2 is shown, a buffer layer 2 has the 1st 20 layer 8 and the 2nd 20 layer 9 in fact.

[0017] the 1st layer 8 -- chemical formula AlxGa1-xN -- it is here, and it comes out and x is formed with the numeric

value of the arbitration which satisfies 0< x<=1, and the ingredient which can be shown. That is, the 1st layer 8 is formed by AlN (alumimium nitride) or AlGaN (gallium nitride aluminum). With drawing 1 and the operation gestalt of drawing 2 , AlN (alumimium nitride) by which x of said formula is equivalent to the ingredient set to 1 is used for the 1st layer 8. The 1st layer 8 is very thin film which has insulation. The 1st lattice constant and coefficient of thermal expansion of a layer 8 are closer to a silicon substrate 1 than the 2nd layer 9.

[0018] the 2nd layer 9 -- GaN (gallium nitride) or chemical formula AlyGa1-yN -- **** to which it is here, and it appears and y changes from y<x, the numeric value of arbitration with which are satisfied of 0< y<1, and the ingredient which can be shown -- it is the thin film. When using the semi-conductor which does not contain the electric conduction form decision impurity which consists of AlyGa1-yN as the 2nd layer 9, in order to prevent a crack with a possibility of generating according to increase of aluminum (aluminum), it is desirable to make y for it to be larger than the value, 0 [i.e.,], with which are satisfied of 0< y<0.8, and smaller than 0.8. In addition, the 2nd layer 9 of this 1st operation gestalt consists of GaN equivalent to y= 0 in the above-mentioned chemical formula. said 2nd layer -- chemical formula AlyGa1-yN -- the numeric value with which y is satisfied of y<x and 0<=y<1 here -- it can also come out and express.

[0019] The desirable thickness of the 1st layer 8 of a buffer layer 2 is 0.5nm - 50nm, i.e., 5-500A. When the thickness of the 1st layer 8 is less than 0.5nm, it becomes impossible to keep good the surface smoothness of the semiconductor region 3 for components formed in the top face of a buffer layer 2. When the thickness of the 1st layer 8 exceeds 50nm, a possibility that a crack may occur is in the 1st layer 8 by hauling distortion which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8.

[0020] The desirable thickness of the 2nd layer 9 is 0.5nm - 200nm, i.e., 5-2000A. When the thickness of the 2nd layer 9 is less than 0.5nm, it becomes difficult to grow up evenly the semiconductor region 3 for components which grows on the 1st layer 8 and a buffer layer 2. Moreover, if the thickness of the 2nd layer 9 exceeds 200nm, with the compressive stress which originates in the stacking fault of the 2nd layer 9 and the 1st layer 8, and is generated in the 2nd layer 9, the electron density of the channel layer 10 will fall and the property of HEMT will deteriorate. Furthermore, it is good preferably to make thickness of the 2nd layer 9 larger than the thickness of the 1st layer 8. If it does in this way, in holding down the distorted magnitude which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8 to extent which a crack does not generate in the 1st layer 9, and maintaining at the concentration-of-electrons high concentration of the channel layer 10, it will become advantageous.

[0021] Next, the manufacture approach of a semi-conductor semiconductor device that the 1st layer 8 was set to AlN and the 2nd layer 9 was set to GaN is explained.

[0022] First, the substrate 1 which consists of p form silicon semi-conductor with which p form impurity shown in (A) of drawing 3 was introduced is prepared. One principal plane 1a of the silicon substrate 1 for forming a buffer layer 2 is a field, i.e., an exact (111) field, just (111) in field bearing of the crystal shown with Miller indices. However, principal plane 1a of a substrate 1 can be made to incline in the range which is shown by 0 in drawing 3 (111) and which is just shown by -theta - +theta to a field. - The range of theta - +theta is -4 degrees - +4 degrees, is -3 degrees - +3 degrees preferably, and is -2 degrees - +2 degrees more preferably. losing the step in the atomic level at the time of carrying out epitaxial growth of a buffer layer 2 and the semiconductor region 3 for components by making just (111) crystal orientation of principal plane 1a of a silicon substrate 1 into a field or (111) the field from a field where an OFF include angle is small -- or it can be made small.

[0023] Next, as shown in drawing 3 (B), the buffer layer 2 on principal plane 1a of a substrate 1 is formed by repeating and carrying out the laminating of the 1st layer 8 which consists of AlN, and the 2nd layer 9 which consists of GaN, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of p form silicon single crystal pretreated by HF system etchant is arranged in the reaction chamber of an MOCVD system, first, thermal annealing for about 10 minutes is performed at 950 degrees C, and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas and NH3 (ammonia) gas are supplied for about 65 seconds in a reaction chamber, and the 1st layer 8 which changes from an AlN layer with a thickness of about 10nm to one principal plane of a substrate 1 is formed. After making whenever [stoving temperature / of a substrate 1] into 1120 degrees C in this example, it is about 63micromol/min and NH3 in the flow rate of TMA gas, i.e., the amount of supply of aluminum. Flow rate 3 of gas, i.e., NH, The amount of supply was made into about 0.14 mol/min. Then,

after making whenever [stoving temperature / of a substrate 1] into 1120 degrees C and stopping supply of TMA gas, it is TMG (trimethylgallium) gas and NH3 in a reaction chamber. Gas (ammonia) is supplied for about 90 seconds, and the 2nd layer 9 which consists of GaN of n form with a thickness of about 30nm is formed in the top face of the 1st layer 8 which consists of the above AlN formed in one principal plane of a substrate 1. At this example, it is about 60micromol/min and NH3 in the flow rate of TMG gas, i.e., the amount of supply of Ga. Flow rate 3 of gas, i.e., NH, The amount of supply was made into about 0.14 mol/min. In this example, 40 layers obtain the buffer layer 2 by which the laminating was carried out in the sum total of the 1st layer 8 which repeats formation of the 1st layer 8 which consists of above-mentioned AlN, and the 2nd layer 9 which consists of GaN 20 times, and consists of AlN, and the 2nd layer 9 which consists of GaN. The 1st layer 8 which consists of AlN, of course, and the 2nd layer 9 which consists of GaN are also changeable into the number of arbitration, such as 50 etc. layers, respectively.

[0024] next, MOCVD of common knowledge on the top face of a buffer layer 2 -- the form semiconductor region 3 for HEMT elements is formed by law. That is, the substrate 1 with which the buffer layer 2 was formed in the top face is arranged in the reaction chamber of an MOCVD system, and they are trimethylgallium gas, i.e., TMG gas, and NH3 first in a reaction chamber. The electronic transit layer 10 which consists of GaN which supplies gas (ammonia) for 15 minutes and does not include un-doping [with a thickness of about 500nm / GaN], i.e., an electric conduction form decision impurity, on the top face of a buffer layer 2 is formed. At this example, it is about 62micromol/min and NH3 in the flow rate of TMG gas, i.e., the amount of supply of Ga. Flow rate 3 of gas, i.e., NH, About 0.23 mols of amount of supply were set to /min.

[0025] Next, the spacer layer 11 which consists of aluminum0.2Ga0.8N which supplies TMG gas and ammonia gas to the TMA gas in a reaction chamber for 85 seconds, and does not include un-doping, i.e., an electric conduction form decision impurity, on the top face of the electronic transit layer 10 is formed in the thickness of 7nm. In this example, about 0.23 mols of flow rates of about 15micromol / min, and NH3 gas were set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to /min for the flow rate of about 8.4micromol/min and TMG gas.

[0026] Next, after interrupting crystal growth for about 15 seconds, the electronic supply layer 12 which supplies TMA gas, TMG gas, ammonia gas, and SiH4 (silane) gas for about 98 seconds in a reaction chamber, and changes from aluminum0.2Ga0.8N to the top face of the spacer layer 11 is formed in the thickness of about 10nm. In this example, about 0.23 mols of flow rates of /min and SiH4 gas were set [the flow rate of the TMA gas at this time / the flow rate of about 8.4micromol/min and TMG gas] to about 21 nmol(s) / min for the flow rate of about 15micromol / min, and ammonia gas.

[0027] Then, the silicon substrate 1 in which the semiconductor region 3 and the buffer layer 2 were formed is taken out from an MOCVD system, and the insulator layer 7 which consists of silicon oxide all over a semiconductor region 3 by well-known plasma CVD is formed. Thickness of an insulator layer 7 is set to about 100nm.

[0028] Although one HEMT is shown in drawing 1 , much HEMT(s) are made to coincidence using one semi-conductor wafer 1, i.e., substrate, at the time of this manufacture. For this reason, with photolithography, a semiconductor region 3 and the component isolation region of a buffer layer 2 are etched to a silicon substrate 1 by reactive ion etching using the mixed gas of 3 boron chloride (BCI3) and hydrogen, and isolation of HEMT is performed. Thus, if isolation is carried out, the electrical characteristics of each component field etc. can be inspected good, without being influenced of other components.

[0029] Next, after using photolithography and fluoric acid system etchant and forming opening for a source electrode and drain electrode formation in an insulator layer 7, using electron beam evaporation etc., laminating formation is carried out one by one, lift off of Ti (titanium) and the aluminum (aluminum) is carried out, and the source electrode 4 and the drain electrode 5 are formed. Also when forming a gate electrode, opening is formed in an insulator layer 7 in the same procedure, and the gate electrode 6 which vapor-deposits and carries out lift off of Pd (palladium), Ti (titanium), and the Au(gold) by electron beam evaporation, and has a function as a shot key barrier electrode is formed. Then, the semiconductor device (HEMT chip) which carried out cutting separation of the epitaxial wafer in the component isolation region, and turned the individual exception according to the well-known dicing process etc. is completed.

[0030] According to HEMT of this operation gestalt, the following effectiveness is acquired.

(1) Since the substrate 1 with which it is low cost and workability also consists of good silicon is used, reduction of ingredient cost and a production cost is possible. For this reason, the cost reduction of HEMT is possible.

(2) The buffer layer 2 which consists of the 1st layer 8 to which the lattice constant formed in one principal plane of a

substrate 1 changes from AlN which has a value between silicon and GaN, and the 2nd layer 9 can succeed the crystal orientation of the substrate 1 which consists of silicon good. Consequently, crystal orientation can be arranged and the GaN system semiconductor region 3 can be formed in one principal plane of a buffer layer 2 good. For this reason, the surface smoothness of a semiconductor region 3 becomes good, and the electrical characteristics of HEMT also become good. When a buffer layer is formed in one principal plane of the substrate 1 which consists of silicon at low temperature only with a GaN semi-conductor, since the difference of a lattice constant is large, silicon and GaN cannot form the GaN system semiconductor region excellent in surface smoothness in the top face of this buffer layer.
(3) As compared with the low-temperature buffer layer which consists of conventional GaN and a monolayer of AlN, crystal growth of the buffer layer 2 which consists of the compound layer of the 1st layer 8 which consists of AlN, and the 2nd layer 9 which consists of GaN can be carried out at an elevated temperature. For this reason, the ammonia used as a nitrogen source can be made to disassemble good, and a buffer layer 2 does not turn into an amorphous layer. For this reason, the consistency of the crystal defect of the epitaxial growth phase 3, i.e., a semiconductor region, formed on a buffer layer 2 can be made small enough, and generating of leakage current can be prevented. Consequently, HEMT with a good pinch-off property can be offered.
(4) Since a substrate 1 is formed from the silicon which is excellent in the heat conductivity as compared with sapphire, the heat generated working [a device] can be made to radiate heat good through a substrate 1, and many properties, such as pressure-proofing of a device and gain, are acquired good.
(5) a silicon substrate 1 -- a nitride system compound semiconductor -- comparing -- since a coefficient of thermal expansion is small -- heat -- it originated irregularly -- pull and distortion joins an epitaxial layer. For this reason, the tensile stress of the interface of AlGaN/GaN between the tooth-space layer 11 and the electronic transit layer 10 can be strengthened further, and the piezo electric field effect can be heightened as a result. For this reason, electron density of the electronic transit layer 10, i.e., a channel, can be made into high concentration as compared with HEMT which used silicon on sapphire, and it becomes possible to decrease the sheet resistance of the electronic transit layer 10, i.e., a channel, and to increase a drain current.
[0031]
[The 2nd operation gestalt] Next, MESFET of the 2nd operation gestalt is explained with reference to drawing 4 . However, in drawing 4 , the same sign is substantially given to the same part with drawing 1 R> 1, and the explanation is omitted. MESFET of drawing 4 prepares n type semiconductor field 3a which consists the semiconductor region 3 of HEMT of drawing 1 of the GaN compound semiconductor layer by which Si was doped as an n form impurity, and forms others identically to drawing 1 . That is, in MESFET of drawing 4 , a silicon substrate 1, a buffer layer 2, the source electrode 4, the drain electrode 5, the gate electrode 6, and the insulator layer 7 are formed like what is shown with the same sign by drawing 1 . N type semiconductor field 3a can also be called a channel layer or a barrier layer, and is arranged on the buffer layer 2. The source electrode 4 and the gate electrode 5 carry out ohmic contact at n type semiconductor field 3a, and are carrying out shot key barrier contact of the gate electrode 6 at n type semiconductor field 3a.
[0032] The manufacture approaches other than GaN semiconductor region 3a of MESFET of drawing 4 are the same as that of the 1st operation gestalt. When forming GaN semiconductor region 3a, TMG gas, NH3 gas, and SiH4 (silane) gas are supplied for about 450 seconds in the reaction chamber used at the time of formation of a buffer layer 2, and with a thickness of about 150nm n type semiconductor field 3a is formed in the top face of the buffer layer 2 formed in one principal plane of a substrate 1. In this example, the flow rate of 0.23 mol/min and SiH4 gas, i.e., the amount of supply of Si, was made [the flow rate of TMG gas, i.e., the amount of supply of Ga] into 21 nmol/min for the flow rate of about 60micromol/min and NH3 gas, i.e., the amount of supply of NH3.
[0033] MESFET of drawing 4 has the same effectiveness as (1) stated in the column of explanation of the effectiveness of HEMT of drawing 1 , (2), (3), and (4). That is, it becomes possible to improve the surface smoothness of making a substrate 1 cheap and semiconductor region 3a, and crystallinity, to improve the property of MESFET, and to radiate the heat of semiconductor region 3a good through a silicon substrate 1.
[0034]
[The 3rd operation gestalt] The configuration of the buffer layer 2 of the 1st and 2nd operation gestalten is changeable. Drawing 5 shows a part of buffer layer 2a which follows the 3rd usable operation gestalt at HEMT, MESFET, etc. Buffer layer 2a of this drawing 5 consists of what carried out the laminating of the 2nd layer 9a of two or more 1st layer 8a and plurality by turns. 1st layer 8a -- chemical formula AlxInyGa1-x-yN -- it is here, and it comes out and x and y

are formed with the numeric value of the arbitration which satisfies 0< x<=1, 0<=y<1, and x+y<=1, and the ingredient which can be shown. That is, 1st layer 8a was chosen from AlN (alumimium nitride), AlGaN (gallium nitride aluminum), AlInN (indium nitride aluminum), and AlGaInN (gallium nitride indium aluminum), and is formed. With the operation gestalt of drawing 5 , aluminum0.5In0.01Ga0.49N equivalent to the ingredient with which x of said formula was set to 0.5, and y was set to 0.01 is used for 1st layer 8a. **** in which 1st layer 8a has insulation -- it is the thin film. The 1st lattice constant and coefficient of thermal expansion containing aluminum of layer 8a have a value between the lattice constant of a silicon substrate 1 and a coefficient of thermal expansion, the lattice constant of semiconductor region 3a, and a coefficient of thermal expansion.

[0035] 2nd layer 9a -- chemical formula AlaInbGa1-a-bN -- it is here and a and b are the numeric value of the arbitration which satisfies 0<=a<1, 0<=b<1, and a+b<=1, and the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9a was chosen from GaN, AlN, InN, InGaN, AlGaN, AlInN, and AlInGaN, and is formed. With the operation gestalt of drawing 5 , aluminum0.05In0.35Ga0.6N equivalent to the ingredient with which a of said formula was set to 0.05, and b was set to 0.35 is used for 2nd layer 9a. It is larger than the band gap of 1st layer 8a, the gap, i.e., the band gap, between the valence band of 2nd layer 9a, and a conduction band.

[0036] Next, 1st layer 8a explains the manufacture approach of buffer layer 2a that aluminum0.5In0.01Ga0.49N and 2nd layer 9a were set to aluminum0.05In0.35Ga0.6N. Buffer layer 2a is formed on principal plane 1a of the same substrate 1 as the 1st operation gestalt. This buffer layer 2a is formed by repeating and carrying out the laminating of 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, and the 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, TMIn (trimethylindium) gas, and NH3 (ammonia) gas are supplied for about 24 seconds in a reaction chamber, and 1st layer 8a which changes from aluminum0.5In0.01Ga0.49N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 1 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 800 degrees C, the flow rate of 47micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas, i.e., the amount of supply of aluminum, / the flow rate of about 14micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 31micromol/min and TMIn gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas, TMG gas, and TMIn gas to 750 degrees C, TMA gas, TMG gas, TMIn gas, and NH3 (ammonia) gas are supplied for about 83 seconds after an appropriate time, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N whose thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8a. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 59micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas / the flow rate of 2.8micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 46micromol/min and TMIn gas. In this example, 1st layer 8a which repeats formation of 1st layer 8a which consists of above-mentioned aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N 10 times, and consists of aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N form the buffer layer 2 by which the 20-layer laminating was carried out by turns. The 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, of course, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N are also changeable into the number of arbitration, such as 50 etc. layers, respectively.

[0037] Since buffer layer 2a of the 3rd operation gestalt of drawing 5 has the same effectiveness as the 1st operation gestalt of drawing 1 and the indium is further contained in buffer layer 2a, it has the effectiveness of the ability to make the coefficient of thermal expansion of buffer layer 2a approximate to a silicon substrate 1 rather than the case where an indium is not included in buffer layer 2a.

[0038]

[The 4th operation gestalt] Buffer layer 2b of the 4th operation gestalt shown in drawing 6 transforms the buffer layer 2 of drawing 1 and drawing 4 , and consists of the crosswise lamination object of the 1st and 2nd layers 8b and 9b. 1st layer 8b -- chemical formula AlxByGa1-x-yN -- it is here, and it comes out and x and y are formed with the numeric value of the arbitration which satisfies 0< x<=1, 0<=y<1, and x+y<=1, and the ingredient which can be shown. That is, 1st layer 8b was chosen from AlN (alumimium nitride), AlGaN (gallium nitride aluminum), AlBN (boron nitride

aluminum), and AlBGaN (gallium nitride boron aluminum), and is formed. With the operation gestalt of drawing 6 , aluminum0.5Ga0.5N equivalent to the ingredient with which x of said formula was set to 0.5, and y was set to 0 is used for 1st layer 8b. 1st layer 8b is very thin film which has insulation. The 1st lattice constant and coefficient of thermal expansion of layer 8b are closer to a silicon substrate 1 than 2nd layer 9b.

[0039] 2nd layer 9b -- chemical formula AlaBbGa1-a-bN -- it is here and a and b are the numeric value of the arbitration which satisfies 0<=a<1, 0<=b<1, and a+b<=1, and the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9b is a layer containing at least one element chosen from aluminum, B, and Ga, and N, for example, was chosen from GaN, BN, AlN, BGaN, AlGaN, AlBN, and AlBGaN, and is formed. With the operation gestalt of drawing 6 , B0.3Ga0.7N equivalent to the ingredient with which a of said formula was set to 0 and b was set to 0.3 is used for 2nd layer 9b. It is larger than the band gap of 1st layer 8b, the gap, i.e., the band gap, between the valence band of 2nd layer 9b, and a conduction band.

[0040] Buffer layer 2b is formed by repeating and carrying out the laminating of 1st layer 8b which consists of aluminum0.5Ga0.5N, and the 2nd layer 9b which consists of B0.3Ga0.7N on principal plane 1a of a substrate 1 which has a field just (111), well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, and NH3 (ammonia) gas are supplied for about 27 seconds in a reaction chamber, and 1st layer 8b which changes from aluminum0.5Ga0.5N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 11 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 1080 degrees C, the flow rate of 31micromol/min and NH3 gas, i.e., the amount of supply of NH3, was set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to about 0.14 mols / min for the flow rate of about 31micromol/min and TMG gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas to 1120 degrees C, TEB (triethyl boron) gas, TMG gas, and NH3 (ammonia) gas are supplied for about 85 seconds after an appropriate time, and 2nd layer 9b which consists of B0.3Ga0.7N of n form where thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8b. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 63micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TEB gas, i.e., the amount of supply of boron,] into about 0.14 mol/min for the flow rate of 75micromol/min and TMG gas, i.e., the amount of supply of a gallium. In this example, 1st layer 8b which repeats formation of 2nd layer 9b which consists of the 1st layer 8b and B0.3Ga0.7N which consists of above-mentioned aluminum0.5Ga0.5N 50 times, and consists of aluminum0.5Ga0.5N, and 2nd layer 9b which consists of B0.3Ga0.7N form buffer layer 2b by which the 100-layer laminating was carried out by turns in total. 1st layer 8b which consists of aluminum0.5Ga0.5N, of course, and 2nd layer 9b which consists of B0.3Ga0.7N are also changeable into the number of arbitration, such as 25 etc. layers, respectively.

[0041] Since buffer layer 2b of drawing 6 has the same effectiveness as the buffer layer 2 of drawing 1 and boron is further contained in 2nd layer 9b, compared with the case where 2nd layer 9b does not contain boron, it becomes strong, and has the effectiveness that generating of a crack can be prevented and 2nd layer 9b can be formed comparatively thickly.

[0042]

[Modification(s)] This invention is not limited to an above-mentioned operation gestalt, and the next deformation is possible for it.

(1) A substrate 11 can be used as silicon compounds, such as polycrystalline silicon other than single crystal silicon, or SiC.

(2) The electric conduction form of each class of semiconductor regions 3 and 3a can be made into an example and reverse.

(3) Each class of semiconductor regions 3 and 3a can be used as the gallium nitride system compound semiconductor or indium nitride system compound semiconductor chosen from GaN (gallium nitride), AlInN (indium nitride aluminum), AlGaN (gallium nitride aluminum), InGaN (gallium nitride indium), and AlInGaN (gallium nitride indium aluminum).

(4) In HEMT of drawing 1 , the electronic supply layer 12 and the same electronic supply layer can be prepared between a barrier layer 10, i.e., an electronic transit layer, and a buffer layer 2.

(5) The insulated-gate mold electrical quantity effectiveness transistor can be prepared instead of HEMT and MESFET.

(6) One layer can make [more] the number of buffer layers 2 and 2a and the 1st layers 8, 8a, and 8b of 2b than the 2nd layer 9, 9a, and 9b, and buffer layers 2 and 2a and the maximum upper layer of 2b can be used as the 1st layer 8, 8a, and 8b. Moreover, the one layer of the number of the 2nd layers 9, 9a, and 9b can also be conversely made [many] rather than the number of the 1st layers 8, 8a, and 8b.
(7) The 1st Layers 8, 8a, and 8b and 2nd layer 9, 9a, and 9b may contain an impurity in the range which does not check these functions.

[Translation done.]

* NOTICES *

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the way, this kind of a gallium nitride system or a nitride system semiconductor device cuts down the wafer which many components made as everyone knows and was full according to dicing, scribing, a cleavage (cleavage), etc., and is formed. Since the insulating substrate which consists of sapphire at this time had the high degree of hardness, it was difficult to perform this dicing etc. with sufficient productivity. Moreover, since sapphire was expensive, the cost of a semiconductor device became high. Moreover, when carrying out crystal growth of the nitride system compound semiconductor on silicon on sapphire, in order to obtain a flat nitride system compound semiconductor layer, it is necessary to form a low-temperature buffer layer as mentioned above. If crystal growth of the nitride system compound semiconductor layer is carried out at an elevated temperature through a low-temperature buffer layer, the comparatively flat nitride system compound semiconductor film can be formed on silicon on sapphire. However, at low temperature, when the low-temperature buffer layer which consists of GaN or AlN is formed, since the ammonia used as a nitrogen source hardly disassembles, a low-temperature buffer layer becomes an amorphous layer containing metal-like Ga and aluminum. Since crystal growth of a channel layer, i.e., the layer of operation etc., is carried out on the buffer layer of this amorphous condition, in the field near a low-temperature buffer layer, the consistency of a crystal defect becomes very high. Since the high field of this defect density functions as an n type semiconductor layer of low resistance, when operating a device, a current leaks it also to this n type semiconductor layer in addition to a layer (channel layer) of operation. Consequently, a good pinch-off property is no longer acquired. As an approach of solving this problem, an AlGaN layer is made to intervene between a buffer layer and a channel layer, and the technique of controlling current leak in a low resistance n type semiconductor layer is proposed by JP,2000-299325,A. However, in order that mediation of an AlGaN layer may generate distortion which originated in the epitaxial layer at the stacking fault, it reduces the electron mobility of a channel layer and invites the problem of making a channel layer generate a crack further etc. For this reason, it was difficult to restrain Al amount and thickness of an AlGaN layer and to fully control leakage current as a result.

[0005] Moreover, the heat conductivity of silicon on sapphire could not fully emit the heat generated working [a device] since it is small, 0.126 W/cm-K and, but caused the fall of many properties of a transistor, such as reducing pressure-proofing, gain, etc. of a device. Furthermore, although the hetero structure which carried out the laminating of the AlGaN is generally adopted on the GaN layer by the GaN system HEMT, when growing up AlGaN on a GaN layer, a stacking fault pulls to the field inboard in AlGaN, and distortion is generated. For this stress, piezo polarization electric field occur in an interface, and if it combines with spontaneous polarization, the electric field of several MV/cm will occur in a hetero interface. Into a channel, it is accumulated by this electric field, the two-dimensional electron gas EG, i.e., 2D, of 1013cm-2 order, the fall of channel sheet resistance is achieved, and a drain current can be made to increase. This is the advantage of the GaN system HEMT which adopted the hetero structure which carried out the laminating of the AlGaN on the GaN layer.

[0006] however, silicon on sapphire -- since a coefficient of thermal expansion is larger than a nitride system compound semiconductor -- heat -- therefore, an epitaxial layer is made to generate a compressive strain irregularly Since this compressive strain works in the direction which cancels the hauling distortion in AlGaN resulting from a stacking fault, it will decrease piezo polarization electric field. For this reason, the concentration of electrons of 2D EG also falls and the engine performance of the AlGaN/GaN system HEMT cannot fully be demonstrated.

[0007] Then, the purpose of this invention is to offer a semiconductor device and its manufacture approaches, such as MESFET using the nitride system compound semiconductor which can solve an above-mentioned trouble, and HEMT.

[Translation done.]

* NOTICES *

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MEANS

[Means for Solving the Problem] This invention for solving the above-mentioned technical problem and attaining the above-mentioned purpose The substrate which is the semiconductor device which has a nitride system compound semiconductor, and consists of silicon or a silicon compound, The semiconductor region for semiconductor devices containing at least one nitride system compound semiconductor layer which has been arranged on one principal plane of said substrate, and has been arranged on a buffer layer and said buffer layer, the 1st main electrode, 2nd main electrode, and control electrode which have been arranged on the front face of said semiconductor region for semiconductor devices -- having -- said buffer layer -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which it is here and said M was chosen from In (indium) and B (boron),

前記x及びyは、 $0<x\leqq 1$、
$0\leqq y<1$、
$x+y\leqq 1$

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula AlaMbGa1-a-bN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

前記a及びbは、 $0\leqq a\leqq 1$、
$0\leqq b<1$、
$a+b\leqq 1$

the numeric value to satisfy and the semiconductor device characterized by consisting of a compound layer with the 2nd layer which comes out and consists of the ingredient shown are started.
[0009] In addition, as shown in claim 2, said 1st layer can be set to AlxGa1-xN, and said 2nd layer can be set to AlaGa1-aN. Moreover, as shown in claim 3, said 1st layer can be made into AlxInyGa1-x-yN, said 2nd layer can be made into AlaInbGa1-a-bN, and In (indium) can be included at least in one side of said 1st and 2nd layers. Moreover, as shown in claim 4, said 1st layer can be made into AlxByGa1-x-yN, said 2nd layer can be made into AlaBbGa1-a-bN, and B (boron) can be included at least in one side of said 1st and 2nd layers. Moreover, as shown in claim 5, as for said buffer layer, it is desirable to consist of said two or more 1st and 2nd layers, and to carry out the laminating of said the 1st layer and said 2nd layer by turns. Moreover, as shown in claim 6, it is desirable for the thickness of said 1st layer in said buffer layer to be [for the thickness of 0.5nm - 50nm and said 2nd layer] 0.5nm - 200nm. As shown in claim 7, as for the principal plane of the side by which said buffer layer of said substrate is arranged, it is desirable that it is the field to which it leans in -4 to +4 times from the field or (111) the field just (111) in field bearing of the crystal shown with Miller indices. Moreover, as shown in claim 8, as for said nitride system compound semiconductor layer, it is desirable to be chosen from a GaN (gallium nitride) layer, an AlInN (indium nitride aluminum) layer, an AlGaN (gallium nitride aluminum) layer, an InGaN (gallium nitride indium) layer, and an AlInGaN (gallium nitride indium aluminum) layer. Moreover, as shown in claim 9, said semiconductor region can be used as two or more semi-conductor layers for forming a field-effect transistor, said 1st main electrode can be used as a source electrode, said 2nd main electrode can be used as a drain electrode, and said control electrode can be used as a gate electrode. Moreover, as shown in claim 10, said semiconductor region can be used as two or more semi-conductor layers for forming a high electron mobility transistor (HEMT). Moreover, as shown in claim 11, said semiconductor region can be used as two or

more semi-conductor layers for forming a metal semiconductor field-effect transistor (MESFET). moreover, the process which prepares the substrate which consists of silicon or a silicon compound in the manufacture approach of a semiconductor device of having a nitride system compound semiconductor as shown in claim 12 and said substrate top -- vapor growth -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which said M was chosen

前記x及びyは、 $0<x\leqq 1$、
$0\leqq y<1$、
$x+y\leqq 1$

from In (indium) and B (boron) here,

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula At least one sort of elements with which said M was chosen from In (indium) and B (boron) AlaMbGa1-a-bN and here,

前記a及びbは、 $0<a\leqq 1$、
$0\leqq b<1$、
$a+b\leqq 1$

it is desirable to have the process which forms the numeric value to satisfy and the 2nd layer which comes out and consists of the ingredient shown one by one, and obtains a buffer layer, the process which forms the semiconductor region for semiconductor devices which consists of at least one nitride system compound semiconductor layer by vapor growth on said buffer layer, and the process which forms the 1st and 2nd main electrodes and control electrodes on the front face of said semiconductor region for semiconductor devices.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is rough **** central drawing of longitudinal section about following [HEMT] the 1st operation gestalt of this invention.
[Drawing 2] It is the top view of HEMT of drawing 1 .
[Drawing 3] It is the sectional view in which expanding the structure of HEMT of drawing 1 in order of a production process, and showing it.
[Drawing 4] It is the sectional view showing MESFET of the 2nd operation gestalt.
[Drawing 5] It is the sectional view showing the substrate of the 3rd operation gestalt, and a part of buffer layer.
[Drawing 6] It is the sectional view showing the substrate of the 4th operation gestalt, and a part of buffer layer.
[Description of Notations]
1 Substrate Which Consists of Silicon Single Crystal
2, 2a, 2b Buffer layer
8, 8a, 8b The 1st layer
9, 9a, 9b The 2nd layer
3 3a Semiconductor region

[Translation done.]

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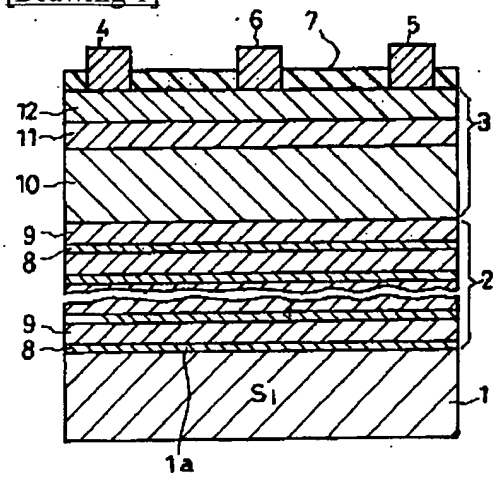
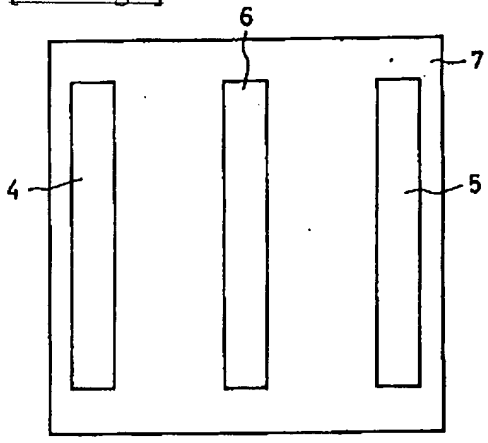
DRAWINGS

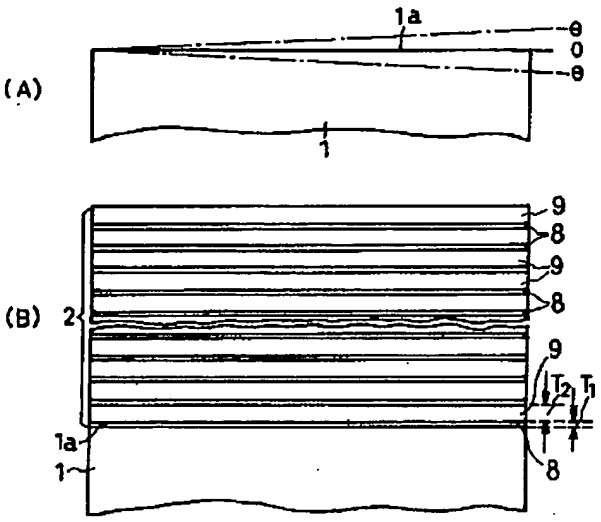
[Drawing 1]



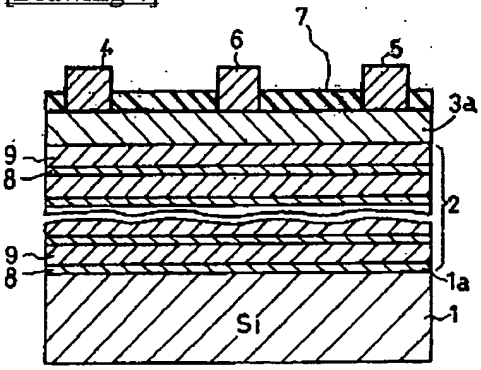
[Drawing 2]



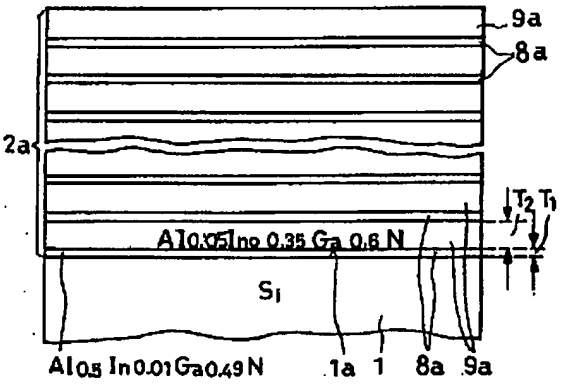
[Drawing 3]



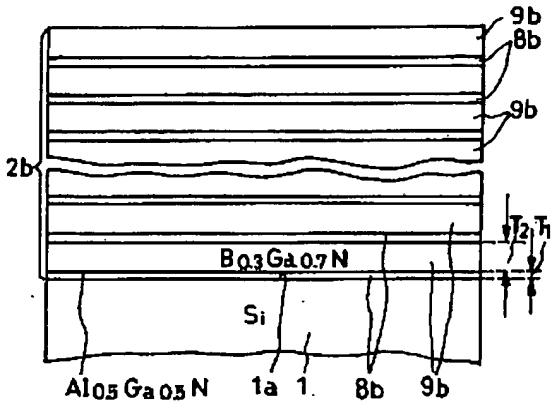
[Drawing 4]



[Drawing 5]



[Drawing 6]



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CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
[Section partition] The 2nd partition of the 7th section
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H01L 21/205
H01L 29/80 B
H01L 29/78 301 B

[Procedure revision]
[Filing Date] October 29, Heisei 16 (2004. 10.29)
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] 0013
[Method of Amendment] Modification
[The contents of amendment]
[0013]
The HEMT element semiconductor region 3 has the electronic transit layer 10 which consists of impurity non-doping GaN, the spacer layer 11 which consists of non-doping aluminum0.2Ga0.8N, and the electronic supply layer 12 which consists of n form aluminum0.2Ga0.8N by which Si is doped as an n form impurity. Each class 10, 11, and 12 of the semiconductor region 3 for components consists of the gallium nitride system compound semiconductor which used nitrogen and a gallium as the base. The electronic transit layer 10 arranged on a buffer layer 2 can also be called a channel layer, and has the thickness of 500nm. It controls that the spacer layer 11 arranged on the electronic transit layer 10 has the thickness of 7nm, and the silicon as an n form impurity of the electronic supply layer 12 diffuses it in the electronic transit layer 10. The electronic supply layer 12 arranged on the spacer layer 11 can also be called a barrier layer, a layer of operation, or a channel layer, and has the thickness of 10nm. The source electrode 4 and the drain electrode 5 carry out ohmic contact at the electronic supply layer 12, and are carrying out Schottky contact of the gate electrode 6 to the electronic supply layer 12. In addition, the high contact layer of n form high impurity

concentration can be prepared between the source electrode 4 and the drain electrode 5, and the electronic supply layer 12. The insulator layer 7 which consists of SiO2 has covered the front face of a semiconductor region 3.
[Procedure amendment 2]
[Document to be Amended] Specification
[Item(s) to be Amended] 0020
[Method of Amendment] Modification
[The contents of amendment]
[0020]
The desirable thickness of the 2nd layer 9 is 0.5nm - 200nm, i.e., 5-2000A. When the thickness of the 2nd layer 9 is less than 0.5nm, it becomes difficult to grow up evenly the semiconductor region 3 for components which grows on the 1st layer 8 and a buffer layer 2. Moreover, if the thickness of the 2nd layer 9 exceeds 200nm, with the compressive stress which originates in the stacking fault of the 2nd layer 9 and the 1st layer 8, and is generated in the 2nd layer 9, the electron density of the channel layer 10 will fall and the property of HEMT will deteriorate.
Furthermore, it is good preferably to make thickness of the 2nd layer 9 larger than the thickness of the 1st layer 8. If it does in this way, in holding down the distorted magnitude which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8 to extent which a crack does not generate in the 1st layer 8, and maintaining at the concentration-of-electrons high concentration of the channel layer 10, it will become advantageous.
[Procedure amendment 3]
[Document to be Amended] Specification
[Item(s) to be Amended] 0031
[Method of Amendment] Modification
[The contents of amendment]
[0031]
[The 2nd operation gestalt]
Next, MESFET of the 2nd operation gestalt is explained with reference to drawing 4. However, in drawing 4, the same sign is substantially given to the same part with drawing 1, and the explanation is omitted.
MESFET of drawing 4 prepares n type semiconductor field 3a which consists the semiconductor region 3 of HEMT of drawing 1 of the GaN compound semiconductor layer by which Si was doped as an n form impurity, and forms others identically to drawing 1. That is, in MESFET of drawing 4, a silicon substrate 1, a buffer layer 2, the source electrode 4, the drain electrode 5, the gate electrode 6, and the insulator layer 7 are formed like what is shown with the same sign by drawing 1. N type semiconductor field 3a can also be called a channel layer or a barrier layer, and is arranged on the buffer layer 2. The source electrode 4 and the drain electrode 5 carry out ohmic contact at n type semiconductor field 3a, and are carrying out shot key barrier contact of the gate electrode 6 at n type semiconductor field 3a.
[Procedure amendment 4]
[Document to be Amended] Specification
[Item(s) to be Amended] 0035
[Method of Amendment] Modification
[The contents of amendment]
[0035]
2nd layer 9a
Chemical formula AlaInbGa1-a-bN
Here, a and b are 0<=a<1,
0<=b<1,
a+b<=1
The numeric value of the arbitration to satisfy,
It is the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9a was chosen from GaN, AlGaN, InGaN, AlGaN, and is used with the operation gestalt of drawing 5, aluminum0.05In0.35Ga0.6N equivalent to the ingredient with which a of said formula was set to 0.05, and b was set to 0.35 is used for 2nd layer 9a. It is smaller than the band gap of 1st layer 8a, the gap, i.e., the band gap, between the valence band of 2nd layer 9a, and a conduction band.

[Procedure amendment 5]
[Document to be Amended] Specification
[Item(s) to be Amended] 0036
[Method of Amendment] Modification
[The contents of amendment]
[0036]
Next, 1st layer 8a explains the manufacture approach of buffer layer 2a that aluminum0.5In0.01Ga0.49N and 2nd layer 9a were set to aluminum0.05In0.35Ga0.6N.
Buffer layer 2a is formed on principal plane 1a of the same substrate 1 as the 1st operation gestalt. This buffer layer 2a is formed by repeating and carrying out the laminating of 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, and the 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, TMIn (trimethylindium) gas, and NH3 (ammonia) gas are supplied for about 24 seconds in a reaction chamber, and 1st layer 8a which changes from aluminum0.5In0.01Ga0.49N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 1 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 800 degrees C, the flow rate of 47micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas, i.e., the amount of supply of aluminum, / the flow rate of about 14micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 31micromol/min and TMIn gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas, TMG gas, and TMIn gas to 750 degrees C, TMA gas, TMG gas, TMIn gas, and NH3 (ammonia) gas are supplied for about 83 seconds after an appropriate time, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N whose thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8a. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 59micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas / the flow rate of 2.8micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 46micromol/min and TMIn gas. In this example, 1st layer 8a which repeats formation of 1st layer 8a which consists of above-mentioned aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N 10 times, and consists of aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N form buffer layer 2a by which the 20-layer laminating was carried out by turns. The 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, of course, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N are also changeable into the number of arbitration, such as 50 etc. layers, respectively.
[Procedure amendment 6]
[Document to be Amended] Specification
[Item(s) to be Amended] 0039
[Method of Amendment] Modification
[The contents of amendment]
[0039]
2nd layer 9b,
Chemical formula AlaBbGa1-a-bN
Here, a and b are $0<=a<1$,
$0<=b<1$,
$a+b<=1$
The numeric value of the arbitration to satisfy,
It is the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9b is a layer containing at least one element chosen from aluminum, B, and Ga, and N, for example, was chosen from GaN, BN, AlN, BGaN, AlGaN, AlBN, and AlBGaN, and is formed. With the operation gestalt of drawing 6, B0.3Ga0.7N equivalent to the ingredient with which a of said formula was set to 0 and b was set to 0.3 is used for 2nd layer 9b. It is smaller than the band gap of 1st layer 8b, the gap, i.e., the band gap, between the valence band of 2nd layer 9b, and a conduction band.
[Procedure amendment 7]

[Document to be Amended] Specification
[Item(s) to be Amended] 0040
[Method of Amendment] Modification
[The contents of amendment]
[0040]
Buffer layer 2b is formed by repeating and carrying out the laminating of 1st layer 8b which consists of aluminum0.5Ga0.5N, and the 2nd layer 9b which consists of B0.3Ga0.7N on principal plane 1a of a substrate 1 which has a field just (111), well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, and NH3 (ammonia) gas are supplied for about 27 seconds in a reaction chamber, and 1st layer 8b which changes from aluminum0.5Ga0.5N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 1 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 1080 degrees C, the flow rate of 31micromol/min and NH3 gas, i.e., the amount of supply of NH3, was set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to about 0.14 mols / min for the flow rate of about 31micromol/min and TMG gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas to 1120 degrees C, TEB (triethyl boron) gas, TMG gas, and NH3 (ammonia) gas are supplied for about 85 seconds after an appropriate time, and 2nd layer 9b which consists of B0.3Ga0.7N of n form where thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8b. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 63micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TEB gas, i.e., the amount of supply of boron,] into about 0.14 mol/min for the flow rate of 75micromol/min and TMG gas, i.e., the amount of supply of a gallium. In this example, 1st layer 8b which repeats formation of 2nd layer 9b which consists of the 1st layer 8b and B0.3Ga0.7N which consists of above-mentioned aluminum0.5Ga0.5N 50 times, and consists of aluminum0.5Ga0.5N, and 2nd layer 9b which consists of B0.3Ga0.7N form buffer layer 2b by which the 100-layer laminating was carried out by turns in total. 1st layer 8b which consists of aluminum0.5Ga0.5N, of course, and 2nd layer 9b which consists of B0.3Ga0.7N are also changeable into the number of arbitration, such as 25 etc. layers, respectively.
[Procedure amendment 8]
[Document to be Amended] Specification
[Item(s) to be Amended] 0042
[Method of Amendment] Modification
[The contents of amendment]
[0042]
[Modification(s)]
This invention is not limited to an above-mentioned operation gestalt, and the next deformation is possible for it.
(1) A substrate 11 can be used as silicon compounds, such as polycrystalline silicon other than single crystal silicon, or SiC.
(2) The electric conduction form of each class of semiconductor regions 3 and 3a can be made into an example and reverse.
(3) Each class of semiconductor regions 3 and 3a can be used as the gallium nitride system compound semiconductor or indium nitride system compound semiconductor chosen from GaN (gallium nitride), AlInN (indium nitride aluminum), AlGaN (gallium nitride aluminum), InGaN (gallium nitride indium), and AlInGaN (gallium nitride indium aluminum).
(4) In HEMT of drawing 1, the electronic supply layer 12 and the same electronic supply layer can be prepared between a barrier layer 10, i.e., an electronic transit layer, and a buffer layer 2.
(5) An insulated gate field effect transistor can be prepared instead of HEMT and MESFET.
(6) One layer can make [more] the number of buffer layers 2 and 2a and the 1st layers 8, 8a, and 8b of 2b than the 2nd layer 9, 9a, and 9b, and buffer layers 2 and 2a and the maximum upper layer of 2b can be used as the 1st layer 8, 8a, and 8b. Moreover, the one layer of the number of the 2nd layers 9, 9a, and 9b can also be conversely made [many] rather than the number of the 1st layers 8, 8a, and 8b.

(7) The 1st Layers 8, 8a, and 8b and 2nd layer 9, 9a, and 9b may contain an impurity in the range which does not check these functions.

[Translation done.]